CLAIMS

1. A method for entering a low power mode, comprising:

providing a first power control mode indicator to a first power control stage, said first power control mode indicator selecting a first low power mode;

receiving a trigger input signal at said first power control stage triggering at least a first module to enter said first low power mode;

providing a first request signal requesting said first module to enter said first low power mode based on said trigger input signal;

providing a first response signal indicating that said first module is ready to enter said first low power mode; and

providing a first control signal in response to said first response signal, said first control signal enabling low power features corresponding to said first low power mode.

2. The method of claim 1, further comprising:

deasserting said first request signal based on said first control signal.

3. The method claim of 1, wherein said first request signal is an interrupt holdoff signal.

4. The method of claim 1, wherein said low power features include at least one of clock gating, reducing voltage, power gating, well biasing, state retention power gating, and dynamic voltage/frequency scaling.

5. The method claim of 4, wherein said first module is a power master.

6. The method of claim 5, wherein said power master is at least one of a microcontroller, digital signal processor, microprocessor, and clock and reset module.

7. The method of claim 6, further comprising enabling at least a portion of said low power features that are internal to said power master based on said first request signal.

8. The method of claim 7, wherein the step of deasserting said first request signal is performed using a first feedback output signal and a first feedback input signal, wherein first feedback output signal is provided by said first power control stage.

9. The method of claim 8, further comprising providing a first trigger output signal to a second power control stage, providing said first feedback input signal using a second feedback output signal, and providing said second feedback output signal using said first trigger output signal.

10. The method of claim 9, wherein said second feedback output signal is provided using a second power control mode indicator corresponding to said second power control stage.

11. The method of claim 10, further comprising providing said second power control mode indicator to said second power control stage, said second power control mode indicator selecting a second low-power mode, receiving said first trigger output signal at said second power control stage triggering at least a second module to enter said second low power mode, providing a second request signal requesting said second module to enter said second low power mode based on said first trigger output signal, providing a second response signal indicating that said second module is ready to enter said second low power mode, providing a second control signal in response to said second response signal, said second control signal enabling said low power features corresponding to said second low power mode, and deasserting said second request signal based on said second control signal.

12. The method of claim 11, wherein said first power control mode indicator and said second power control mode indicator are tied to a node.

13. The method of claim 11 wherein said second module is one of a display controller, a graphics controller, a camera sensor interface, a video encoder, a video decoder, a direct memory access controller, USB, or any other type of accelerator.

14. The method of claim 11, wherein said first low power mode and said second low power mode are at least one of a WAIT mode, a STOP mode, a DOZE mode, and a Deep Sleep Mode (DSM).

15. An apparatus for entering a low power mode, comprising:

a first module;

a first power control stage coupled to said first module;

a first power control mode indicator provided to said first power control stage, said first power control mode indicator selecting a first low power mode;

a trigger input signal received at said first power control stage triggering at least said first module to enter said first low power mode;

a first request signal requesting said first module to enter said first low power mode, said first request signal based on said trigger input signal;

a first response signal indicating that said first module is ready to enter said first low power mode; and

a first control signal provided in response to said first response signal, said first control signal enabling low power features corresponding to said first low power mode, wherein said first request signal is deasserted based on said first trigger input signal.

16. The apparatus of claim 15, wherein said first module is a power master being at least one of a microcontroller, digital signal processor, , and microprocessor, said low power features include at least one of clock gating, reducing voltage, power gating, well biasing, state retention power gating, and dynamic voltage/frequency scaling, and said low power mode is at least one of a WAIT mode, a STOP mode, a DOZE mode, and a Deep Sleep Mode (DSM).

17. The apparatus of claim 16, wherein said deassertion is performed using a first feedback output signal and a first feedback input signal, wherein first feedback output signal is provided by said first power control stage.

18. The apparatus of claim 17, wherein said first power control stage provides a first trigger output signal to a second power control stage, and said first feedback input signal is generated using said first feedback output signal and a second feedback output signal corresponding to said second power control stage, wherein said second feedback output signal is generated using said first trigger output signal.

19. The method of claim 18, wherein said second feedback output is generated using a second power control mode indicator corresponding to said second power control stage.

20. An apparatus for entering a low power mode, comprising:

a first power control stage, said first power control stage receiving a first input signal and generating a first request signal based on said first input signal; and

a first module coupled to said first power control stage, wherein said first module receives said first request signal and provides a first response signal in response to receiving said first request signal, said first response signal indicating that said first module is ready to enter a first low power mode, said first low power mode being predicated by a mode indicator, said first power control stage providing a first control signal in response to said first response signal, said first request signal being deasserted based on said first control signal.

21. The apparatus of claim 20, wherein said first module is a power master, said first request signal is an interrupt holdoff, said first request signal being deasserted is based on a first feedback output signal and a feedback input signal, and said first feedback output signal is provided by said first power control stage.